Addendum A1 to TPC/MPD TDR, rev.07

Front-End Electronics based on PASA and ALTRA chips

Laboratory of High Energy Physics, JINR
Dubna 2018

1 FEE Design concept and general requirements

The Front-End Electronics (FEE) has to read out charge detected by pads of the readout chamber located at the TPC end-caps. These pads deliver a current signal with a fast rise time and a long tail due to the motion of the positive ions. The induced on the pad plane signal is usually over 3 neighbouring pads.

To satisfy the NICA project requirements, the TPC's data readout system has to transfer the mean data stream of 7 GBps with the mean multiplicity per event of about 300 tracks and maximum multiplicity up to 1000 tracks. Another significant condition is to minimize the quantity of the substance in the TPC end-caps.

The 16-channel ALICE TPC chip set (PASA [**1**] and ALTRO [**2**]) was adopted in FEC design to amplify the low noise signal to provide data processing and zero suppression. Another essential component of the system is FPGAs which provide communication and control functions. The data from all FECs are readout in parallel via fast serial interfaces. Readout Control Units (RCUs) are equipped with optical links.

The main parameters of the front-end electronics for TPC are specified in **Table 1**.

Table 1: Main parameters of FEE

Parameter	**Value**
Total number of channels	95 232
Signal to noise ratio, S/N	$>$ 30:1 @ MIP ($\sigma_{noise} < 1000$ e$^-$)
Dynamic Range	1000 (10-bit sampling ADC)
Shaping time	180-190 ns
Sampling	10 MHz
Tail cancellation	$<$ 1% (after 1 μs)
Zero-suppression	up to 90%
Bandwidth	up to 5 GB/s @ TPC
Power consumption	100 mW/ch

Each of the two end-caps of the TPC is divided into 12 readout chambers (see Chapter 4). The readout system of each chamber is independent. Every readout chamber (ROC) is served by 62 FECs having 64-channels each and one RCU as it is shown in **Fig.1**.

Thus, all the data readout system consists of 95 232 registration channels, 1488 FECs and 24 RCUs.

2 Front-end card and its prototype

2.1 Prototype card

The first phase of the FEE development was to create front-end card prototype (FEC64) for the ALTRO features study and the FPGA logic debugging. This card has interface

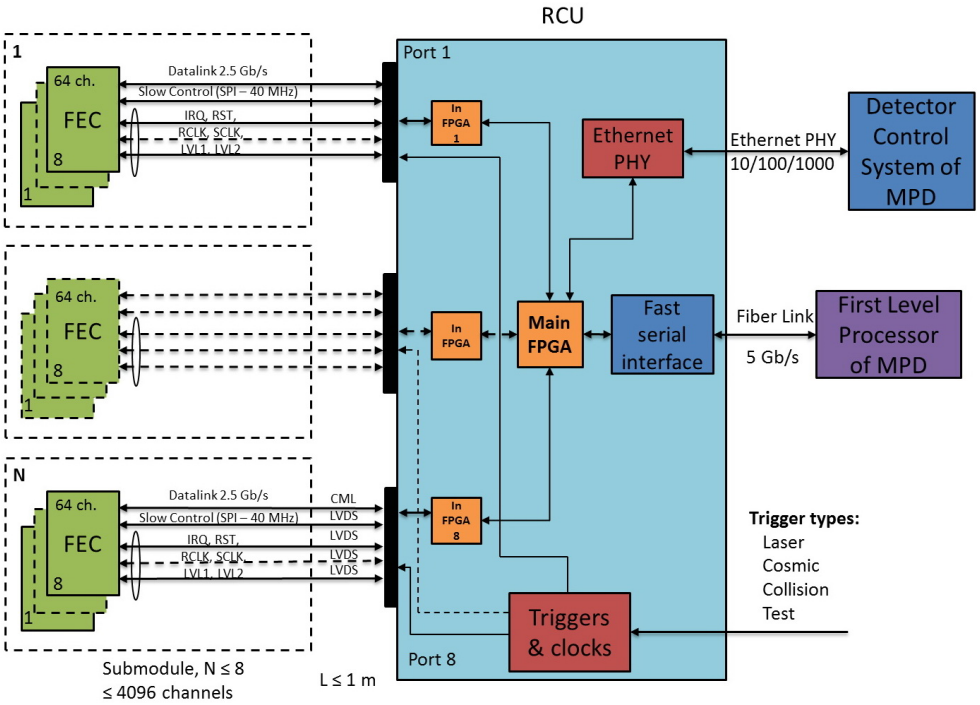

Figure 1: Structural scheme of one chamber readout

USB 2.0 that allows you to operate with it without readout controller (RCU). The structural scheme of prototype card FEC64 is shown in **Fig.2**.

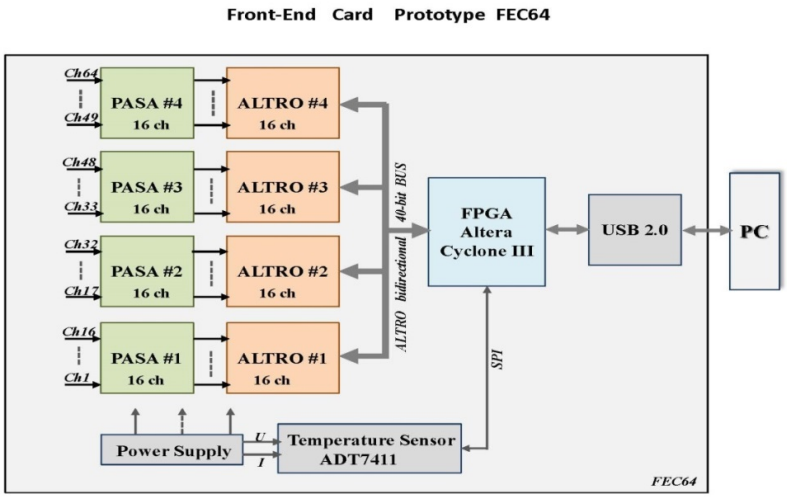

Figure 2: FEC-prototype block-diagram

On the FE card, as was FE-prototype, there are 4 PASAs and 4 ALTROs supporting altogether 64 channels per board and one FPGA Altera that performs the functions of the controller.

The FPGA architecture is shown in **Fig.3**.

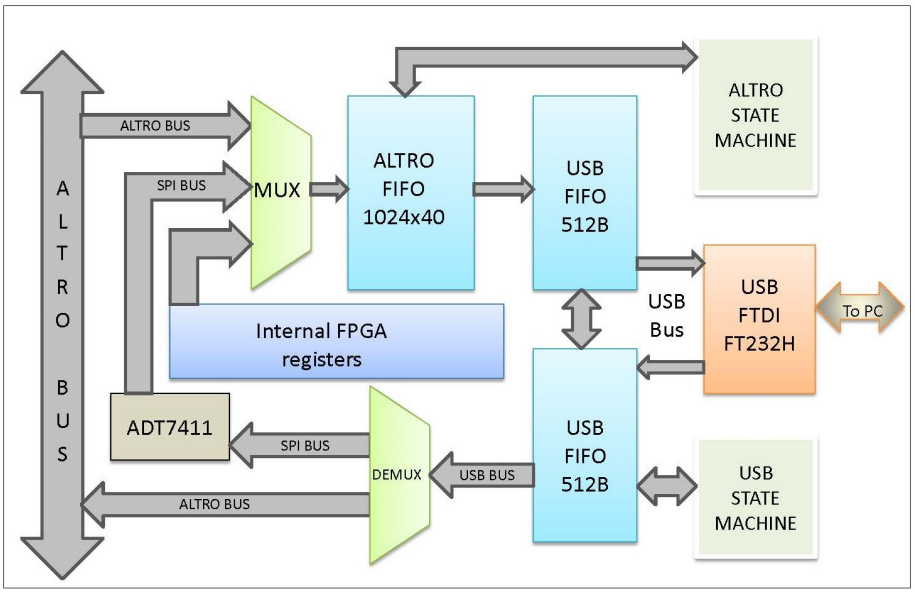

Figure 3: FPGA architecture

The main tasks of FPGA are clock and power supply control, trigger signal control, interfaces with 40-bit bi-direction bus of ALTRO chip, SPI-bus and with FT232H (USB 2.0).

2.2 Front-end card FEC64S

The 64-channel front-end card FEC64S [**4**] is a modified version of the prototype card FEC64. Like the prototype it consists of 64 readout channels and based on two ASICs: Pre Amplifier ShAper (PASA) and the ALice Tpc ReadOut chip (ALTRO chip).

The card FEC64S view and its structural scheme are shown in **Figs.4** and **5**.

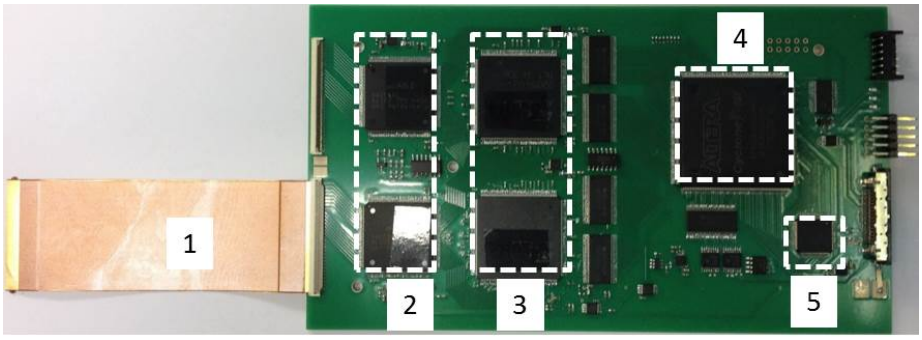

Figure 4: Front-End Card FEC64S. 1) Cable between the detector and FEC; 2) PASA chips - low noise amplification of the signal; 3) ALTRO chips - digitization and processing; 4) FPGA board controller; 5) Serializer/Deserializer chip

The signal flow starts with the analogue signal transported through two flexible cables and connectors at the detector end. The PASA has short connection links to these connectors to minimize the crosstalk caused by the fast input signal from detector. Afterwards, the ALTROs are directly joint to the PASAs using differential

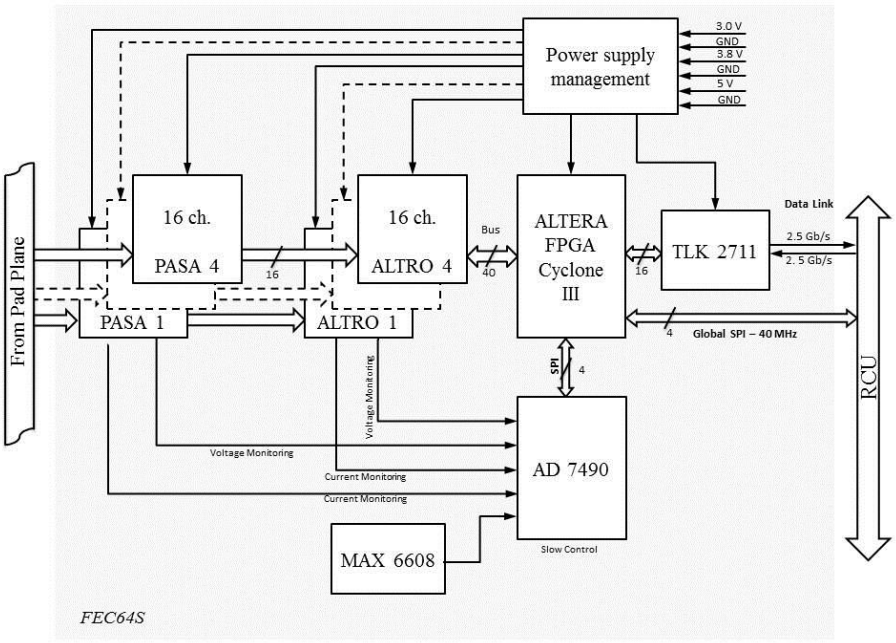

Figure 5: Card FEC64S structural scheme

signals. The ALTRO chip connects the analogue part of the FEC64S with the digital part. The digital outputs are multiplexed through the LVCMOS (Low Voltage CMOS) bus, which is connected to the FPGA.

The main function of FPGA is multiplexing 40-bit ALTRO words to a serial stream which is transmitted through a high-speed transceiver of the TLK 2711 chip (1.6÷2.5 Gbps).

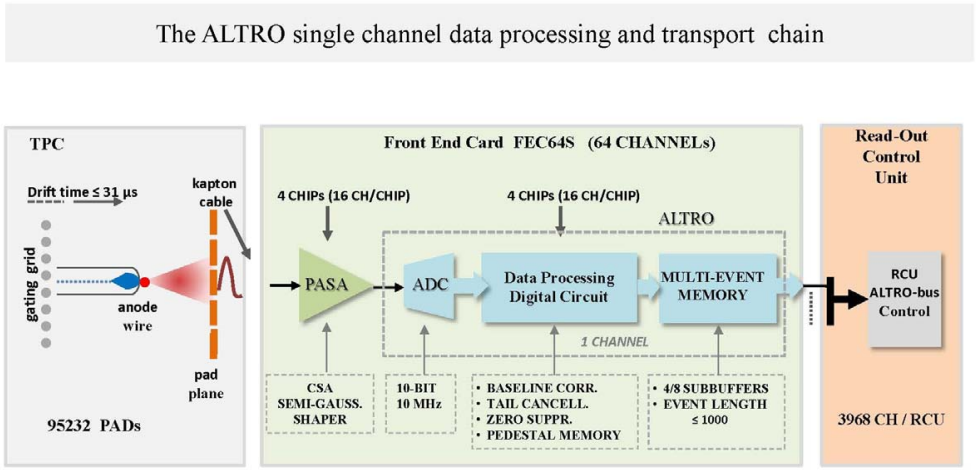

Figure 6: Single channel structural scheme

The scheme of one registering channel is shown in **Fig.6**. The output signals of the PASA chip are digitized by a 10-bit pipeline ADC with 25 MSps (one per channel) operating at a configurable sampling rate in the range of 2.5-25 MHz. After the analogue to digital conversion, the signal processing is performed in 5 steps: 1) the

first correction and substraction of the signal baseline, 2) the cancellation of long-term components of signal tail, 3) the second baseline correction, 4) the suppression of the samples having no useful information (zero suppression) and 5) data formatting. The ADC and digital processing logic are contained in the ALTRO as well as the buffer memory for 4-8 events. The digital processing parameters are configurable from the detector control system.

The vital component of the FEC is ALTERA EP3C16Q240 FPGA. The on-board FPGA implements the following functions:

- assures a possibility of initialzing all ALTROs channels;
- provides the acquisition modes;
- reformats 40-bit ALTROs words to 10-bit words for consequent coding;
- encodes outgoing ALTROs data with Hamming-code;
- monitors the condition of the FEC and collects some statistic information;
- provides managment of the FEC;
- realizes the auxiliary slow control interface - SPI (Serial Peripheral Interface) 40 MHz.

The card can operate in two acquisition modes. They are the individual readout mode (IRM) and automatic scan mode (ASM). In IRM RCU has to send Channel Readout command individually to all channels to receive the data contained there. This mode is fairly slow and does not allow receiving the information simultaneously from all FECs.

The ASM is used for automation of the data readout process. After activating of ASM the FEC becomes the master. In this mode the FPGAs state machine monitors the arrival of the second level trigger (LVL2) which informs that the valid data are stored in the ALTRO buffer memory. After receiving of LVL2 the FPGAs state machine starts to read the event length registers of all the ALTRO channels and stores their information in the dedicated FIFO memory. When the event length information is received from all 64 channels, the data readout circuit becomes active. At this ASM mode only the channels which actually have buffered the data are read out and all the empty channels are skipped.

It is worth noting that receiving the event length information is of higher priority than the channel readout in the FPGAs state machine. This is done because the event length register contains the information only about the latest event stored in the ALTRO buffers while for ADC samples there is the multi-event buffer memory. The data readout cycle from the channels is interrupted if another LVL2 has been obtained before all the available information is received and the cycle is resumed only after the new event length information is stored to the dedicated FIFO memory in the FPGA.

After receiving Channel Readout command the ALTRO becomes the master of the bus and starts to transfer the registered ADC data from the multi-event buffer. In the ALTRO transfer mode the transmission of 40-bits data words starts at every cycle of the readout clock. The received parallel data are stored in a specialized FIFO buffer. The data at the FIFO output are sliced up in 10-bit words and then coded with Hamming

code. The 11-th bit at the Hamming coder input is used for informational coloring of the words being transmitted. The 16-bit output words of the Hamming coder are given to the parallel input of Serializer/Deserializer chip TLK2711 to be serialized and transmitted to RCU.

Also FPGAs firmware implements the functions of monitoring conditions of the board. Every FEC contains the 12 bit 16 channels - ADC AD7490 of successive approximation which is connected to the FPGA via SPI (Serial Peripheral Interface). An analogue temperature sensor MAX6607 is connected to one of the ADC channels. The measurement range of sensor is from -20°C to +85 °C and accuracy from 0.6 °C to 1.5 °C.

The remaining 15 channels are used for measuring currents and voltages. The measured values of currents, voltages and temperature of the board are taken to the FPGA where they are compared with the threshold registers. When the threshold is violated the interruption line is set and the interruption vector is formed.

ALTROs and PASAs are combined on the card into two groups. Each of these groups is fed from separate power sources which are managed from FPGA. This architecture allows one to switch off half of the board if some problem occurs.

A set of 62 registers has been realized in FPGA firmware.They are needed to manage the card, monitor its state and collect some statistics. The access to the FPGA registers is available through the high-speed serial interface as well as through additional SPI 40 MHz. The SPI slave has been realized in FPGA and can be used optionally.

The SRAM based FPGA on FECs are particularly sensitive to radiation exposure because they will be located directly on the ROCs. The option of cyclic redundancy checking of the firmware is activated to prevent the incorrect operation of FPGA caused by violation of its configuration file. If any error occurs the FPGA activates the CRC line and external circuit initializes its reconfiguration.

The FECs PCB (Printed Circuit Board) contains four signal layers and four power layers divided into two supply layers and two ground layers. The FEC64S is 95 mm wide and 167 mm long.

3 FEC testing

When developing the FEC it is necessary to control noise and crosstalk values which affect the chamber space and dE/dx resolutions. The Equivalent Noise Charge (ENC) was calculated by means of measuring the signal RMS value at the absence of the injected charge. To improve the measurement precision, we have taken the average value of several ten thousand measurements.

The measured value of ENC for all the channels turned out to be about 0.5 ADC bits (see **Fig.7**).

In order to measure FEC linearity, the input charge was generated by using a voltage step into the capacitor connected in series with the input. As a voltage source we used the Keysight 81160A pulse generator with remote control. To decrease the signal amplitude, the attenuator was connected to the generator output. The **Fig.8** shows a typical response curve. The crosstalk was studied as well. It was found to be about 0.5 %.

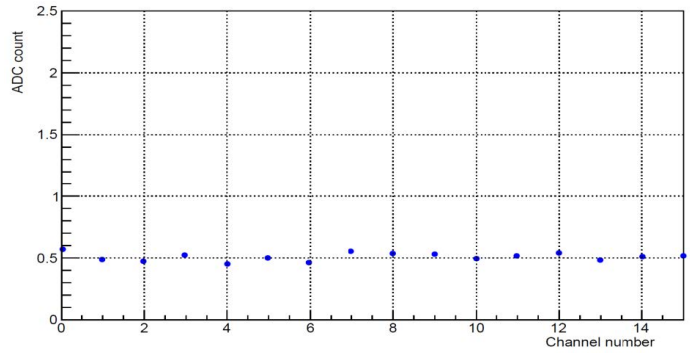

Figure 7: Noise value at 16 FECs channels (without cable)

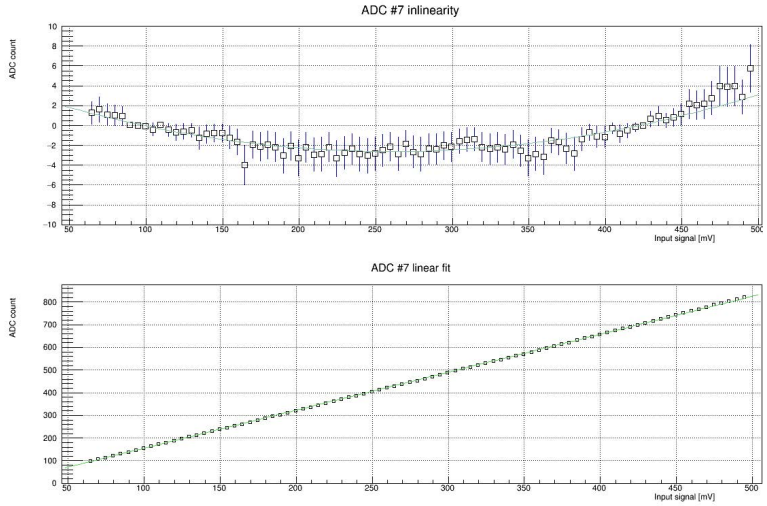

Figure 8: FEC linearity. Top graph shows the difference between the measured value and the linear fit. The bottom graph demonstrates FEC response to the input signal

4 Readout control unit

The RCU fulfils key system-level functions: distribution of trigger and clock signals to the FECs, configuration of each front-end channel, readout of the trigger related data from the FECs, subsequent formatting and transfer to the MPD DAQ system. RCU also provides monitoring the voltages, currents, board temperature and acquisition status registers.

RCU is based on ALTERA Cyclone V GX series FPGAs. It consists of 8 input FPGAs and one main FPGA. Each of 8 input FPGAs serves up to 8 FECs. Up to 64 FECs can be connected to the RCU.

Each input FPGA receives a serial stream from FECs implemented through the embedded high-speed transceivers. After data deserialization by FPGA which then decodes the information by Hamming code, reformats it to the 32-bits and stores to each of 8 FIFO buffers.

All the 8 input channels operate simultaneously. When the information from the cards is received then it is multiplexed and transmitted to the main FPGA through the high-speed transceiver.

The general task of the main FPGA is receiving and multiplexing the data from

Figure 9: Test system for eight cards. 1) FECs array (512 ch. in total), 2) clocks and control signal distribution card, 3) RCU emulator

8 input FPGAs. The multiplexed data stream is transmitted to a high-speed optical link. Additionally to the optical interface the main FPGA is equipped with Ethernet of 10/100/1000 which provides independent link with the MPD detector control system.

At this point the RCU schematic has been completed. The FPGA firmware has been designed and tested. The PCB design is in progress.

In our design the FECs are directly connected to the RCU. The RCU emulator based on Cyclone V SX development board was used to test the FECs that also allowed one to verify RCUs FPGA firmware. The **Fig.9** shows a test setup. The setup consists of Cyclone V SX development board, 8 FECs (512 ch. in total), power supply sources and the dedicated card made to fan-out triggers, clocks and reset signals.

5 Data stream estimate

The estimated evaluation of data stream from front-end electronics which is replaced at the readout chambers of TPC was calculated on the basis of initial parameters from **Table 2**.

The results of calculation on data stream estimate for 300 tracks are given in **Table 3**.

Table 2: Initial parameters for data stream estimate

Parameter	**Value**
Total number of channels	95 232
Pad raw number per ROC	53
ADC bit digitization	10
Event header size per channel (bit)	40
Time-stamp and cluster width size (bit)	20
Frequency of events (kHz)	7
Average number of tracks in TPC	300
Maximal number of tracks in TPC	1000

Table 3: Data stream estimate for 300 tracks

Parameter	**Value**
Event size without filtering (Mbit)	303
Front-end input stream (Gbps)	2121
Throughput of one FEC64S (Gbps)	2
Total throughput of Front-end (Gbps)	3024
Event size with filtering (Mbit)	7

References

[1] ALICE TPC Electronics. Charge Sensitive Shaping Amplifier (PASA) Technical Specifications.

[2] ALICE TPC Readout Chip. User Manual. CERN, June 2002, Draft 0.2. ALTRO chip web page, [http://ep-ed-alice-tpc.web.cern.ch/ep-ed-alice-tpc].

[3] Averyanov A. et. al. Readout system of TPC/MPD NICA project. Nuclear Physics and Engineering, Physics of Atomic Nuclei, 2015, Vol.78, No.13, pp. 1556-1562.

[4] S.Vereshchagin et al., Front-end Readout electronics of TPC MPD/NICA, Conference-school of Young Scientists and Specialists of JINR Alushta'13, June 3-8th, 2013, Alushta, Russia.

[5] S.Vereshchagin et al., Readout electronics for TPC MPD/NICA, Young Scientists and Specialists of JINR Alushta'14, June 2-7th, 2014, Alushta, Russia.

[6] S.Vereshchagin et al.Front-end readout electronics for TPC/MPD-NICA, International Conference-Session of the Section of Nuclear Physics of PSD RAS, 17-21 November 2014, National Research Nuclear University MEPhI, Moscow, Russia, (in Russian).

[7] G.Cheremukhina, S.Movchan, S.Vereschagin and S.Zaporozhets. Front-End Electronics development for TPC detector in the MPD/NICA project.// JINST (2017), 066P-0517 v.1

[8] G.Cheremukhina, S.Movchan, S.Vereschagin and S.Zaporozhets. Readout Electronics for the TPC Detector in the MPD/NICA Project. // Proceedings of Inter-

national Conference on Technology and Instrumentation in Particle Physics 2017. Springer Proceedings in Physics 212. Volume 1. pp. 195 200, 2018.

List of Figures

List of Tables